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Low Power Consumption Using CMOS VLSI Design in Modern Trends

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ABSTRACT

The revolution of wireless communication, portable and mobile devices has consistently demanding the designer to design the device for low power consumption. Power loss becomes a main parameter of integrated circuits, particularly for portable computers and personal communication systems. There has been consistent research and development to improve the power consumption and performance of the device in various level of abstraction starting from mask layout – circuit, Gate and Register level- to system level. Various approaches including hardware and software are identified to design the VLSI Circuit with minimum power consumption and optimization between the power and performance. This paper analyzes the main source of power indulgence in CMOS circuit & their impact.

KEY WORDS: Static dissipation, Dynamic dissipation, Power-Delay.

1. INTRODUCTION

Methods: The CMOS power indulgences are static and dynamic. When there is no transition in logic. Dynamic power dissipation occurs when there is a transition of logic from high to low or vice versa. Main source of power indulgence in chip is due to dynamic power indulgence. The dynamic power is dissipated in the form of charging, discharging of capacitance.

With advent in semiconductor technology especially in the last few years there has been drastic revolution in the field of information and technology. Tens of million of transistor are fabricated in a single chip. At the same time the complexity in designing, testing and fabricating the chip has also increased. The major worry for the designer now is to optimize the power consumption without degrading the performance.

Dynamic power dissipation is summation of P-switching & S-short-circuit.

$P_{switching} = a\ f\ Ceff\ .Vdd^2$

$S_{short\text{-}circuit} = I_{sc}\ .Vdd.f.$

We introduce the CMOS inverter and observe the various parameters and their impact in power dissipation.

CMOS Inverter:

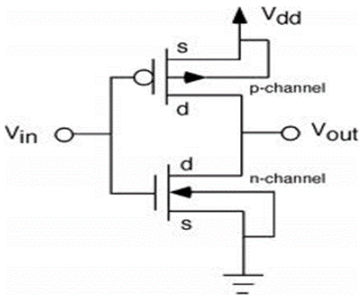

Figure.1. CMOS Inverter

Observation of key parameters and their impact on power and delay for cmos inverter are purposed below based on simulation

Clock frequency and its impact on power dissipation: The fundamental dynamic power dissipation equation $\mathbf{P = \alpha CV^2F}$ shows that the power dissipation depends on load capacitance clock frequency and supply voltage. An experimental setup fig (2) to show a linear relation between clock frequency and the power consumption is carried out. We verify this here by simulating the inverter over a frequency range (0.5 GHz, 1GHz, and 1.5 GHz). A capacitor of 10fF is used as a load.

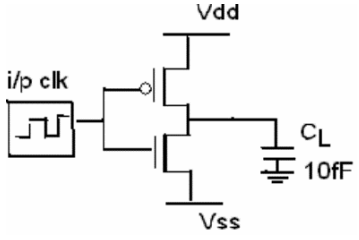

Figure.2. Inverter Connected to Various Clock Frequencies

The observation is shown in the figure 3.as the clock frequency increases so does the power consumption**.** This shows the linear dependency of clock frequency and the power consumption. To have a better performance of

device it is necessary to increase the clock frequency especially for high speed device but in the mean time optimization is sought for low power consumption.

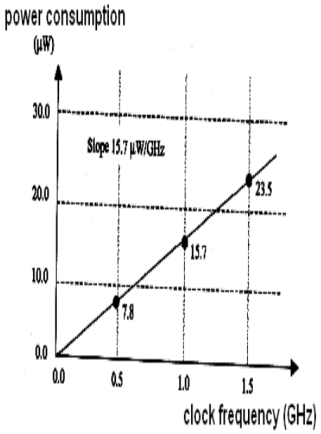

Figure.3. Clock Vs Power consumption

Load capacitance and its impact on power dissipation: To obtain the effect of output capacitance and delay of cmos inverter a layout is drawn based on .12 micron cmos technology with a inverter connected with single inverter and with four inverters as shown in figure 4.

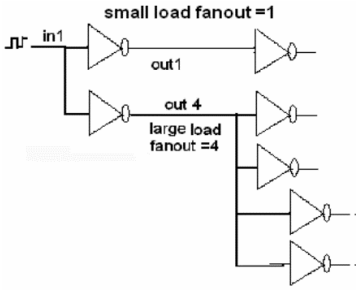

Figure.4. Inverter Connected with another Inverter of Fanout 1 and Fanout 4

The inverter with small load capacitance (fanout=1) has fast switching and with large output capacitance (fanout=4) has slow switching characteristics. This observation is made true by simulating the inverter with different load capacitance and deriving the rise and fall time. The average of rise and fall time gives the switching time.

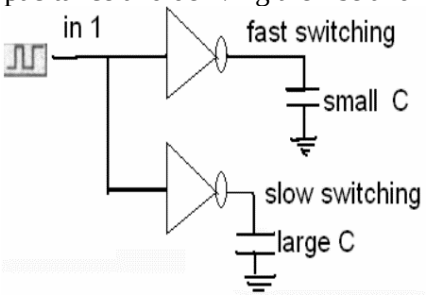

Figure.5. Fan In/Out Switching

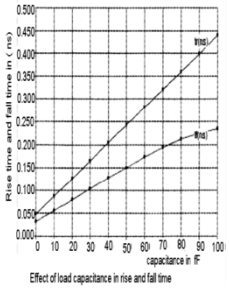

Figure.6. Graphical representation of fan In and Fan OUT

The figure 6 shows that as the load capacitance is increased rise and fall time also increase.

Supply voltage and its impact on power dissipation: The equation P=_CV2F suggest that there is a quadrature effect of supply voltage in power dissipation as it is proportional to square of the supply voltage. A first order approximation shows that the power consumption is proportional to V_{dd2} .The experiment is conducted by using the supply voltage from 0.5v to 2V with supply voltage increment step as 0.1V.the graph plotted below shows that the square law is valid 0.8v to 1.5v .there is a very rise in power consumption after 1.5v due to the avalanche effect in n channel MOS device. It is necessary to figure out the optimization between the supply voltage and the performance of the device. For this delay dependency in supply voltage is shown in figure 8.

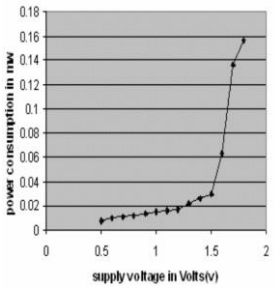

Figure.7. Increase in Power Consumption with Vdd

The delay significantly increases as the supply voltage is scaled from 1.6 v .eventually after 0.7v the delay is such a high the simulator does not evaluate and device does not work.

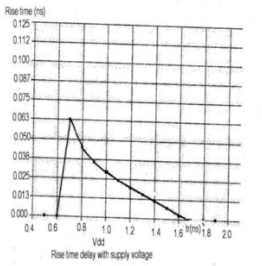

Figure.8. Rise time delay with supply voltages

2. CONCLUSION

The paper has revisited the major dynamic power dissipation components and studied the impact on cmos inverter hence it gives a better idea to optimize the power and performance of the design. The result and plots were obtained by simulation.

REFERENCES

Brintha Rajakumari S, Nalini C, An efficient data mining dataset preparation using aggregation in relational database, Indian Journal of Science and Technology, 7, 2014, 44-46.

Etienne Sicard, Sonia Delmas, Basics of Cmos celldesign, Tata McGraw-hill, 2005.

International roadmap for semiconductor, 2005

Jayalakshmi V, Gunasekar N.O, Implementation of discrete PWM control scheme on Dynamic Voltage Restorer for the mitigation of voltage sag swell, International Conference on Energy Efficient Technologies for Sustainability, ICEETS, 2013, 1036-1040.

Kaliyamurthie K.P, Parameswari D, Udayakumar R, QOS aware privacy preserving location monitoring in wireless sensor network, Indian Journal of Science and Technology, 6 (5), 2013, -4648-4652.

Kaliyamurthie K.P, Udayakumar R, Parameswari D, Mugunthan S.N, Highly secured online voting system over network, Indian Journal of Science and Technology, 6 (6), 2013, 4831-4836.

Khanaa V, Thooyamani K.P, Saravanan T, Simulation of an all optical full adder using optical switch, Indian Journal of Science and Technology, 6 (6), 2013, 4733-4736.

Khanaa V, Thooyamani K.P, Using triangular shaped stepped impedance resonators design of compact microstrip quad-band, Middle - East Journal of Scientific Research, 18 (12), 2013, 1842-1844.

Kumaravel A, Dutta P, Application of Pca for context selection for collaborative filtering, Middle - East Journal of Scientific Research, 20 (1), 2014, 88-93.

Raj M.S, Saravanan T, Srinivasan V, A modified direct torque control of induction motor using space vector modulation technique, Middle - East Journal of Scientific Research, 20 (11), 2014, 1572-1574.

Saravanan T, Raj M.S, Gopalakrishnan K, VLSI based 1-D ICT processor for image coding, Middle - East Journal of Scientific Research, 20 (11), 2014, 1511-1516.

Sengottuvel P, Satishkumar S, Dinakaran D, Optimization of multiple characteristics of EDM parameters based on desirability approach and fuzzy modeling, Procedia Engineering, 64, 2013, 1069-1078.

Sundararajan M, Optical instrument for correlative analysis of human ECG and breathing signal, International Journal of Biomedical Engineering and Technology, 6 (4), 2011, 350-362.

Thamotharan C, Prabhakar S, Vanangamudi S, Anbazhagan R, Anti-lock braking system in two wheelers, Middle - East Journal of Scientific Research, 20 (12), 2014, 2274-2278.

Udayakumar R, Khanaa V, Saravanan T, Saritha G, Retinal image analysis using curvelet transform and multistructure elements morphology by reconstruction, Middle - East Journal of Scientific Research, 16 (12), 2013, 1781-1785.

Vanangamudi S, Prabhakar S, Thamotharan C, Anbazhagan R, Design and fabrication of dual clutch, Middle - East Journal of Scientific Research, 20 (12), 2014, 1816-1818.

Vanangamudi S, Prabhakar S, Thamotharan C, Anbazhagan R, Design and calculation with fabrication of an aero hydraulwicclutch, Middle - East Journal of Scientific Research, 20 (12), 2014, 1796-1798.

Weste N, Eshraghian K, principles of CMOS VLSI design, Addison Wesley, International roadmap for Semiconductors, 1993.